L Number	Hits	Search Text	DB	Time stamp
1	113	distribute$1 with input with buffer$1 with switch$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 17:54
2	1	(central with arbit$7) same (distribute$1 with input with buffer$1 with switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 17:53
3	3	(central with arbit$7) and (distribute$1 with input with buffer$1 with switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 18:09
4	22	distribute$1 near5 input near5 buffer$1 near5 switch$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 17:55
5	3	(central with arbit$7) and (distribute$1 near5 input near5 buffer$1 near5 switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 18:10
6	1	(distribute$1 near5 input near5 buffer$1 near5 switch$3) same pipeline$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 18:10
7	941	370/$.ccls. and 710/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 18:10
8	1	(370/$.ccls. and 710/$.ccls.) and (distribute$1 with input with buffer$1 with switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 18:11
-	265	double near5 fifo	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/05 12:14
-	1	(arbitrat$4 near5 request$3) same (double near5 fifo)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/05 12:16
-	715	(arbitrat$4 near5 request$3) same switch$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/05 12:17
-	1	(double near5 fifo) and ((arbitrat$4 near5 request$3) same switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/05 12:34
-	59	central same ((arbitrat$4 near5 request$3) same switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/05 12:35

L Number	Hits	Search Text	DB	Time stamp
1	113	distribute$1 with input with buffer$1 with switch$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 17:54
2	1	(central with arbit$7) same (distribute$1 with input with buffer$1 with switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 17:53
3	3	(central with arbit$7) and (distribute$1 with input with buffer$1 with switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 18:09
4	22	distribute$1 near5 input near5 buffer$1 near5 switch$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 17:55
5	3	(central with arbit$7) and (distribute$1 near5 input near5 buffer$1 near5 switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 18:10
6	1	(distribute$1 near5 input near5 buffer$1 near5 switch$3) same pipeline$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 18:10
7	941	370/$.ccls. and 710/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 18:10
8	1	(370/$.ccls. and 710/$.ccls.) and (distribute$1 with input with buffer$1 with switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/06 18:11

09/749,795

US-PAT-NO: 6208644

DOCUMENT-IDENTIFIER: US 6208644 B1

TITLE: Network switch providing dynamic load balancing

DATE-ISSUED: March 27, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pannell; Donald Robert	Cupertino	CA	N/A	N/A
Hemming; Robert Donald	Ben Lomond	CA	N/A	N/A

US-CL-CURRENT: 370/389, 370/392 , 370/400 , 370/422

ABSTRACT:

A network switch routes data transmissions between network stations, each data transmission including network addresses of the source and destination network stations. The network switch includes a set of input/output (I/O) ports each for receiving data transmissions from and transmitting data transmissions to a subset of the network stations. Each I/O port is identified by a "physical" port ID and a "logical" port ID. While each I/O port's physical port ID is unique, all I/O ports that can route data to the same subset of network stations share the same logical port ID. Each I/O port receiving a data transmission from a network station sends its logical port ID and the network addresses included in the data transmission to an address translation system. The address translation system uses data in the translation request to maintain a lookup table relating each subset of network addresses to a logical port ID identifying all I/O ports that communicate with network stations identified by that subset of network address. The address translation system responds to an address translation request by returning the logical port ID of all I/O ports that can send data transmissions to a destination station identified by the destination address included in the data transmission. In response to the returned logical port ID, the network switch establishes a data path for the data transmission from the I/O port receiving the data transmission and any idle I/O port having that logical port ID.

10 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 11

---------- KWIC ---------

Brief Summary Text - BSTX (5):

Networks transfer data between computers or other types of network stations. For example 10BASE-T Ethernet systems use sets of twisted pair conductors to connect network stations to a **central** hub or **switch**. A network **switch** includes input ports for receiving data packets from various network sources, output ports for forwarding packets to various network destinations and a **switching** mechanism such as a crosspoint **switch** for selectively routing each incoming packet from an input port to the appropriate output port. The network **switch** also includes an address translation system which relates a network destination address included in each incoming packet to an output port that can forward the

packet to that network address. When an input port receives an incoming packet it stores the packet, reads its network destination address, consults the address translation system to determine which output port is to forward the packet, and then sends a routing **request to the switch's arbitration** system. When the **arbitration system determines that the requested** output port is idle it establishes a connection through the crosspoint **switch** between the requesting input port and the requested output port and then notifies the input port that it may begin sending the packet to the output port via the crosspoint **switch**.

US-PAT-NO: 6185203

DOCUMENT-IDENTIFIER: US 6185203 B1

TITLE: Fibre channel switching fabric

DATE-ISSUED: February 6, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Berman; Stuart B.	Newport Beach	CA	N/A	N/A

US-CL-CURRENT: 370/351, 370/360

ABSTRACT:

The Fibre Channel standard was created by the American National Standard for Information Systems (ANSI) X3T11 task group to define a serial I/O channel for interconnecting a number of heterogeneous peripheral devices to computer systems as well as interconnecting the computer systems themselves through optical fiber and copper media at gigabit speeds (i.e., one billion bits per second). Multiple protocols such as SCSI (Small Computer Serial Interface), IP (Internet Protocol), HIPPI, ATM (Asynchronous Transfer Mode) among others can concurrently utilize the same media when mapped over Fibre Channel. A Fibre Channel Fabric is an entity which transmits Fibre Channel frames between connected Node Ports. The Fibre Channel fabric routes the frames based on the destination address as well as other information embedded in the Fibre Channel frame header. Node Ports are attached to the Fibre Channel Fabric through links.

59 Claims, 34 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 23

---------- KWIC ---------

Brief Summary Text - BSTX (19):

In one aspect of the invention, the apparatus comprises separate port control modules, one for each attached device, a **central** router module, a **switch** core module, a fabric control module and a brouter (bridge/router) module. In the preferred embodiment, the port control modules are connected to the router modules by separate route request connections and separate route response connections. Through this structure, route requests may be provided from the port control module to the router while simultaneously the router provides route request responses to the same port control module. Preferably, a common route request channel is utilized. Thus, apparatus is provided to return a route response to a previously **requesting port while other ports are arbitrating and sending route requests** to the centralized router. More generally, this apparatus provides for reading resource requests from multiple requesters while at the same time returning resource grant responses to previous requesters.

US-PAT-NO: 6154799

DOCUMENT-IDENTIFIER: US 6154799 A

TITLE: Repeater-switch for distributed arbitration digital data buses

DATE-ISSUED: November 28, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gafford; Thomas Austin	Redondo Beach	CA	N/A	N/A
Eross, deceased; Botond Gabor	late of Palo Alto	CA	N/A	N/A
Moorer, legal representative;	San Rafael	CA	N/A	N/A
by James A.	San Rafael	CA	N/A	N/A
Barrie, legal representative;				
by Barbara L.				

US-CL-CURRENT: 710/107, 710/119

ABSTRACT:

The technical field of the invention generally concerns digital computers and, in particular, repeaters or switches (40) for distributed arbitration digital data buses (52, 54, 56, and 58) to which devices (62, 64, 66, 68, 72 and 74) connect in parallel. The bus repeater/switch (40) includes a plurality of bus interface cards (48) that are connected to the distributed arbitration buses (52, 54, 56 and 58) for receiving signals from and transmitting signals to devices (62, 64, 66, 68, 72 and 74) connected thereto. The bus interface cards (48) connect to a control card (44) which allows signals from one of the sharing buses (52, 54 or 56) to be exchanged with the shared bus (58). The bus switch (40) also includes selector switch (84 or 88) for choosing which particular one of the sharing buses (52, 54 or 56) exchanges digital data signals with the shared bus (58). The bus switch (40) responds to signals on the distributed arbitration buses (52, 54, 56 and 58) and to phases of the protocol for those signals so that its presence between pairs of buses (52-58, 54-58 or 56-58) is imperceptible to devices (62, 64, 66, 68, 72 and 74) connected thereto.

13 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

---------- KWIC ---------

Brief Summary Text - BSTX (27):

Thus far, bus **switches** for arbitration type buses exist only for multi-master centralized arbitration buses. In such **central arbitration, requests for access to the bus come to a single arbitration** circuit. These **requests to the arbitration** circuit may be presented on several different bus

request signal lines that respectively correspond to different priority levels for the requesting devices. Multiple devices may be connected to the same wire-OR bus request signal line. When such bus **request signals arrive at the central arbitration** circuit, it decides when and to which priority level it will grant control of the bus. The result of the arbitration circuit's decision is then transmitted back to the devices via bus grant signal lines included in the bus. In these **central** arbitration buses, the bus grant signal lines are often daisy-chained through the devices connected to the bus so the first requesting device at a particular priority level can block retransmission of the grant signal to devices further along the bus from the **central** arbitration circuit, and thereby take control of the bus. This daisy-chaining and grant blocking, if present, is sometimes described a positional priority system.

Brief Summary Text - BSTX (28):

With these **central arbitration buses, since the bus request signals flow to the central arbitration** circuit and the bus grant signals flow from that circuit, it is relatively straight forward to build a bus **switch** that passes them between one of several sharing buses and the shared bus. By sensing whether the bus request signal and the bus grant signal pass through the **switch,** it can determine the proper direction to drive the bus control lines. Moreover, by sensing which of the two interconnected buses produces the data strobe signal and whether a read or write is occurring, the bus **switch** can decide in which direction to drive the data lines.

US-PAT-NO: 6061330

DOCUMENT-IDENTIFIER: US 6061330 A

TITLE: Flow and congestion control in packet switched networks

DATE-ISSUED: May 9, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Johansson; Per Gunnar	Hagersten	N/A	N/A	SE

US-CL-CURRENT: 370/229, 370/230

ABSTRACT:

A control system in an ATM system controls flows of data cells and flow control management cells from a number of sources to a destination over connections passing a network element. The flow control management cells are returned from the destination via the network element to their respective sources. The network element is exposed to congestion due to contention between the connections, that necessitates queuing of the connections. The flow control management cells have an explicit rate field for an explicit rate value used to limit a source maximum allowed cell rate to a specific value. An operating function uses deviations from an available rate value for lower priority cells and from a queue length reference forming a desirable queue length, to calculate a modified explicit rate value as a function of these deviations. This modified explicit rate value is introduced into the explicit rate field of the backward flow control management cells.

24 Claims, 21 Drawing figures

Exemplary Claim Number: 9

Number of Drawing Sheets: 8

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Detailed Description Text - DETX (29):

A typical **switch solution with distributed buffering has, as mentioned above, large input buffers** at the input ports and relatively small buffers at the output ports. Cell losses in the small output buffer are avoided by means of an internal flow control mechanism, which does not form part of the invention. Furthermore, to avoid head of line blocking, the input buffers should be logically divided into separate buffers for each output port. The distribution of buffering means that the actual offered rate and queue will be spread between the input buffers, but the algorithm must operate with the total rate and queue length in order to cope with the fairness objectives. A way to attain this, schematically illustrated in FIG. 2, is to let a switch internal cell format convey counts of arrived cells and measures or queue lengths from each logical input buffer to an output port, where the actual explicit rate calculation and backward RM cell assignment takes place.

US-PAT-NO: 5872787

DOCUMENT-IDENTIFIER: US 5872787 A

TITLE: Distributed switch buffer utilizing cascaded modular switch chips

DATE-ISSUED: February 16, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Cooperman; Michael	Framingham	MA	N/A	N/A
Sieber; Richard	Attleboro	MA	N/A	N/A

US-CL-CURRENT: 370/412, 370/429

ABSTRACT:

A distributed switch buffer and method for switch buffer enlargement use standard switch chips as modules that are cascaded in multiples to provide arbitrarily large switch buffers for any number of inputs and outputs. Any type of packet switch chip may be used in any combination. A packet that enters the first switch chip in the cascade automatically gets transferred to other switch chips as part of an integrated buffering scheme. Every input of the switch is connected to all of the switch chips in the first stage of the distributed buffer. The queue of each output of the switch is then expanded by adding more stages of switch chips. All outputs of each switch chip go to the inputs of the same switch chip in the next stage of the distributed buffer so that all of the buffer space of all the cascaded switch chips is available to each input port. The queue may be expanded indefinitely by cascading more chips. In one embodiment, inputs are connected to all the cascaded switch chips for each output port so that each chip only needs to have one output. The number of inputs for each switch chip in the intermediate stages need not equal the number of outputs from that stage, and it is possible to use a different number of cascade stages for each switch output port.

12 Claims, 3 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

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Drawing Description Text - DRTX (2):
FIG. 1 is a logical block diagram of a 4-**input, 4-output 3-stage distributed switch buffer** according to the present invention;

Drawing Description Text - DRTX (4):
FIG. 3 is an alternate embodiment, utilizing only single-output chips, of a 4-**input, 4-output 3-stage distributed switch buffer** according to the present invention.

Detailed Description Text - DETX (4):

In the embodiment of FIG. 1, four inputs 2 enter the first stage 4 of the distributed switch buffer, connecting at all of the first-stage 4X1M switch chips 6, 8, 10, 12. Every **input of the switch is connected to all of the switch chips in the distributed buffer** first stage 4. Each switch chip output port 14 has a queue size of K packets. The queue of each output 32 of the switch is then expanded by adding more stages of 4X1M chips of the same type, where M signifies that multiple packets are read out in one time slot. The outputs 14 of each first stage 4 switch chip enter the second stage 16, in such a manner that the outputs 14 from each first stage 4 switch chip enter the same second-stage 16 switch chip, i.e. the outputs 14 from switch chip 6 all enter switch chip 18, the outputs 14 from switch chip 8 become the inputs for switch chip 20, and so on for the remaining second-stage switch chips 22, 24. The second-stage 16 switch chips of this implementation are also all 4X1M chips.

DERWENT-ACC-NO: 1996-506531

DERWENT-WEEK: 199952

TITLE: ATM switch with traffic control system performing cell **switching and distribution control - has input and output buffer memories storing cells at each of several input and output ports which switches and distributes cells input** from input ports to output ports by main body of switch

INVENTOR: FUKANO, M; NAKAGAWA, T ; YAMADA, K

PATENT-ASSIGNEE: NEC CORP[NIDE]

PRIORITY-DATA: 1995JP-0092217 (April 18, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
AU 9650726 A	October 31, 1996	N/A	028	H04L 012/56
AU 710694 B	September 30, 1999	N/A	000	H04L 012/56
JP 08288953 A	November 1, 1996	N/A	007	H04L 012/28
US 5774453 A	June 30, 1998	N/A	000	H04L 012/56

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
AU 9650726A	N/A	1996AU-0050726	April 17, 1996
AU 710694B	N/A	1996AU-0050726	April 17, 1996
AU 710694B	Previous Publ.	AU 9650726	N/A
JP 08288953A	N/A	1995JP-0092217	April 18, 1995
US 5774453A	N/A	1996US-0633214	April 16, 1996

INT-CL (IPC): H04L012/28, H04L012/56 , H04Q003/00

ABSTRACTED-PUB-NO: AU 9650726A

BASIC-ABSTRACT:

The ATM switch includes an output buffer corresponding to each output port, which stores cells to be output to the output port. A logical queue contains several first priority queues for storing cells depending on the traffic priority indicated by the cell input to the output buffer. An idle queue supervises the remaining capacity of the logical queue to be used. It also generates several overflow signals corresponding to several predetermined threshold values of remaining capacity depending on defining congestion states of output buffer.

The ATM switch also contains an input buffer corresponding to each input port,

for storing cells to be output to the main body of the switch. The input buffer includes several second logical queues corresponding to each of the output ports and each containing several second priority queues for storing calls depending on the traffic priority indicated by the cell input to the input buffer. A controller stops cell output from the second priority queues which have predetermined traffic priority corresponding to the congestion state represented by the overflow signal, unless other higher second priority queues contain no cell to be output.

ADVANTAGE - Performs cell switching and distribution in accordance with degree of priority cell and congestion state of system.

ABSTRACTED-PUB-NO: US 5774453A

EQUIVALENT-ABSTRACTS:

The ATM switch includes an output buffer corresponding to each output port, which stores cells to be output to the output port. A logical queue contains several first priority queues for storing cells depending on the traffic priority indicated by the cell input to the output buffer. An idle queue supervises the remaining capacity of the logical queue to be used. It also generates several overflow signals corresponding to several predetermined threshold values of remaining capacity depending on defining congestion states of output buffer.

The ATM switch also contains an input buffer corresponding to each input port, for storing cells to be output to the main body of the switch. The input buffer includes several second logical queues corresponding to each of the output ports and each containing several second priority queues for storing calls depending on the traffic priority indicated by the cell input to the input buffer. A controller stops cell output from the second priority queues which have predetermined traffic priority corresponding to the congestion state represented by the overflow signal, unless other higher second priority queues contain no cell to be output.

ADVANTAGE - Performs cell switching and distribution in accordance with degree of priority cell and congestion state of system.

CHOSEN-DRAWING: Dwg.1/2

TITLE-TERMS: ATM SWITCH TRAFFIC CONTROL SYSTEM PERFORMANCE CELL **SWITCH DISTRIBUTE CONTROL INPUT OUTPUT BUFFER MEMORY STORAGE CELL INPUT OUTPUT PORT SWITCH DISTRIBUTE CELL INPUT** INPUT PORT OUTPUT PORT MAIN BODY SWITCH

DERWENT-CLASS: W01

EPI-CODES: W01-A03B1; W01-A06E1; W01-A06G2;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1996-426758

US-PAT-NO: 5838937

DOCUMENT-IDENTIFIER: US 5838937 A

TITLE: Data transmitting/receiving method using distributed path control in data switching system

DATE-ISSUED: November 17, 1998

INVENTOR-INFORMATION: NAME	CITY	STATE	ZIP CODE	COUNTRY
Lee; Hyeun Tae	Daejeon	N/A	N/A	KR
Lee; Keun Woo	Daejeon	N/A	N/A	KR

US-CL-CURRENT: **710/316**, **370/351** , **370/360**

ABSTRACT:

A data transmitting/receiving method using **distributed** path control in a data **switching** system is disclosed, including the steps of: (1) storing data by distributing a first code and a last code of a received data frame, and then reading and storing a frame header; requesting a path setting and then initializing a trial number; transmitting a setup request signal in the next time slot with a destination port address if a polling address is its own address, and thus transmitting the stored header through a data channel when the response signal received from the destination output port indicates an end of the path controlling operation; and transmitting data stored in an **input buffer** to the end of a frame and requesting a path release at its polling address; (2) releasing the path in case of path release request when the destination port address is its own port address; if the output port is not in use, the output **buffer** is not is a full state, and a communication channel is available, indicating the end of the path controlling operation in a response bus in case of the path setup request and receiving a **switch** path setup data to discriminate an initial code and last code of the frame, thereby transmitting the data.

4 Claims, 10 Drawing figures

Exemplary Claim Number: 4

Number of Drawing Sheets: 10

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Abstract Text - ABTX (1):

A data transmitting/receiving method using **distributed** path control in a data **switching** system is disclosed, including the steps of: (1) storing data by distributing a first code and a last code of a received data frame, and then reading and storing a frame header; requesting a path setting and then initializing a trial number; transmitting a setup request signal in the next time slot with a destination port address if a polling address is its own address, and thus transmitting the stored header through a data channel when the response signal received from the destination output port indicates an end of the path controlling operation; and transmitting data stored in an **input buffer** to the end of a frame and requesting a path release at its polling address; (2) releasing the path in case of path release request when the

destination port address is its own port address; if the output port is not in use, the output **buffer** is not is a full state, and a communication channel is available, indicating the end of the path controlling operation in a response bus in case of the path setup request and receiving a **switch** path setup data to discriminate an initial code and last code of the frame, thereby transmitting the data.

Current US Original Classification - CCOR (1):
710/316

Current US Cross Reference Classification - CCXR (1):
370/351

Current US Cross Reference Classification - CCXR (2):
370/360